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PTO/SB/21 (09-06)
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(to be used for all correspondence after initial filing)

Application Number	10/085,164
Filing Date	February 26, 2002
First Named Inventor	Stephen G. Kelly
Art Unit	2814
Examiner Name	Pham, Hoai V.
Attorney Docket Number	A539WTN
Total Number of Pages in This Submission	33

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☑ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
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- ☐ Petition
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Jackson Walker L.L.P.		
Signature			
Printed name	Christopher J. Rourk		
Date	January 22, 2007	Reg. No.	39,348

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/085,164	Confirmation No. 8036
Applicants	:	Kelly et al.	
Filed	:	February 26, 2002	
Title:	:	ENCAPSULATED DIE PACKAGE WITH IMPROVED PARASITIC AND THERMAL PERFORMANCE	
Art Unit	:	2814	
Examiner	:	Pham Hoai V.	
Docket No.	:	A539WTN	

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APPELLANT'S BRIEF (37 C.F.R. 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on November 17, 2006 (received by the U.S. Patent and Trademark Office on November 20, 2006) and the Final Office Action mailed July 25, 2006.

The fees required under § 1.17(c), and any required petition for extension of time for filing this brief and related fees are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

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The final page of this brief bears the practitioner's signature.

I REAL PARTIES IN INTEREST (37 C.F.R. §41.37(c)(1))

The real party in interest in this appeal is:

☒ the following party:

Microsemi Corporation, by Assignment recorded with the U.S. Patent and Trademark Office on April 29, 2002 at Reel 012847, Frame 0554.

II RELATED APPEALS AND INTERFERENCES

(37 C.F.R. §41.37(c)(2))

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal:

A ☒ there are no such appeals or interferences.

III STATUS OF CLAIMS (37 C.F.R. §41.37(c)(3))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 65

B. STATUS OF ALL THE CLAIMS IN APPLICATION

Claims rejected: Claims 1-18, 20-35 and 37-43

Claims withdrawn: Claims 51-65

Claims cancelled: Claims 19, 36 and 44-50

C. CLAIMS ON APPEAL

The claims on appeal are: Claims 1-18, 20-35 and 37-43

IV STATUS OF AMENDMENTS (37 C.F.R. 41.37(c)(4))

An amendment was submitted subsequent to the final rejection of the claims to claim 40 to correct the antecedent basis for a claim term as noted by the Examiner in the final Office action. Entry of the amendment was refused by the Examiner, who asserts that the "extensive changes to the claim 40 would require search and reconsideration of the proposed amended claim."

V SUMMARY OF THE CLAIMED SUBJECT MATTER (37 C.F.R. 41.37(c)(5))

Claim 1 includes a packaged semiconductor device that comprises a semiconductor die, a substrate with the semiconductor die disposed therein, and a plurality of leads coupled to the semiconductor die, wherein at least one said lead has a shaped end proximate the substrate and configured to minimize parasitic capacitance over a predetermined frequency range. An encapsulant encloses the semiconductor die and plurality of leads, the encapsulant having a consistant dielectric constant over the predetermined frequency range. The encapsulant is operable to shunt thermal capacitance and thermal resistance away from the semiconductor die. By way of example and not by limitation, see Figures 1-3 and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0021] and [0024].

Claim 2 includes the packaged semiconductor device as recited in Claim 1, further comprising an I/O common terminal, at least one input terminal and at least one output terminal, coupled to the semiconductor die. By way of example and not by limitation, see Figures 1-3 and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0021] and [0024].

Claim 3 includes the packaged semiconductor device as recited in Claim 2, wherein the input terminal(s) and output terminal(s) are positioned orthogonal to the I/O common terminal. By way of example and not by limitation, see Figures 1-3 and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0021] and [0024].

Claim 4 includes the packaged semiconductor device as recited in Claim 3, wherein the semiconductor die is positioned above the I/O common terminal. By way of example and not by limitation, see Figures 1-3 and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0021] and [0024].

Claim 5 includes the packaged semiconductor device as recited in Claim 4, wherein the encapsulant forms a substantially hexagonal structure surrounding the I/O common terminal, input terminal(s), and output terminal(s), essentially at right angles with respect to the substrate. By way of example and not by limitation, see Figures 1-3 and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0021] and [0024].

Claim 6 includes the packaged semiconductor device as recited in Claim 5, further comprising a lead-frame for coupling the input terminal(s) to a circuit and the output terminal(s)

to a circuit. By way of example and not by limitation, see Figures 1-3 and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0021] and [0024].

Claim 7 includes the packaged semiconductor device as recited in Claim 6, wherein the portion of the lead-frame coupled to each of the input terminal(s) and output terminal(s) possess exposed dovetailed side edges operable to allow epoxy to lock on the sides and top of the exposed edges. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 8 includes the packaged semiconductor device as recited in Claim 3, further comprising an end surface of the input terminal(s) being positioned adjacent and parallel to the side surface of the I/O common terminal, and an end surface of the output terminal(s) being positioned adjacent and parallel to the opposing side surface of the I/O common terminal, said end surfaces being shaped so as to minimize parasitic capacitance. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 9 includes the packaged semiconductor device as recited in Claim 1, wherein the configured lead has a rounded shape expanding outward toward the substrate. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 10 includes the packaged semiconductor device as recited in Claim 8, further comprising length and width dimensions of approximately .079 millimeters and .065 millimeters, respectively, and a height dimension of approximately .032 millimeters. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 11 includes the packaged semiconductor device as recited in Claim 8, further comprising an operating frequency range from DC to 10 gigahertz. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 12 includes the packaged semiconductor device as recited in Claim 8, further comprising use in a surface mount assembly. By way of example and not by limitation, see

Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 13 includes the packaged semiconductor device as recited in Claim 8, further comprising use in an integrated circuit. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 14 includes the packaged semiconductor device as recited in Claim 8, further comprising use in an amplifier gain stages. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 15 includes the packaged semiconductor device as recited in Claim 8, further comprising metallization, including a first and second metallization strip, as the means of coupling the input terminal(s) and the output terminal(s) to the semiconductor die. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 16 includes the packaged semiconductor device as recited in Claim 15, further comprising a path length from input terminal to the output terminal, of a fraction of the wavelength for which frequency the semiconductor device is designed. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 17 includes the packaged semiconductor device as recited in Claim 8, further comprising bond wires as the means of coupling the input terminal(s) and the output terminal(s) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire, a second end of the first bond wire being coupled to the semiconductor die, a first end of a second bond wire being coupled to the semiconductor die, a second end of the second bond wire being coupled to the output terminal. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 18 includes the packaged semiconductor device as recited in Claim 17, further comprising a path length from the input terminal to the output terminal of a fraction of the wavelength for which frequency the semiconductor device is designed. By way of example and

not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C and 7B of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0024].

Claim 20 includes the packaged semiconductor device as recited in Claim 1, further comprising a light emitting semiconductor as the semiconductor die. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 21 includes the packaged semiconductor device as recited in Claim 20, further comprising a light emitting diode as the light emitting semiconductor. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 22 includes the packaged semiconductor device as recited in Claim 20, further comprising a substantially clear epoxy material as the encapsulant. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 23 includes the packaged semiconductor device as recited in Claim 20, further comprising a cathode and an anode as the plurality of leads. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 24 includes the packaged semiconductor device as recited in Claim 23, further comprising the positioning of the cathode and the anode opposite to each other. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 25 includes the packaged semiconductor device as recited in Claim 24, further comprising an encapsulant with a substantially hexagonal structure around the cathode and the anode essentially at right angles with respect to the substrate. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 26 includes the packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the cathode. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 27 includes the packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the cathode operable to minimize parasitic capacitance. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 28 includes the packaged semiconductor device as recited in Claim 27, further comprising a rounded shape on the end surface of the cathode. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 29 includes the packaged semiconductor device as recited in Claim 23, further comprising metallization as the cathode coupling means to the semiconductor die. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 30 includes the packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the cathode to the semiconductor die, a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 31 includes the packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the anode. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 32 includes the packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the anode operable to minimize parasitic capacitance. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 33 includes the packaged semiconductor device as recited in Claim 32, further comprising a rounded shape on the end surface of the anode. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 34 includes the packaged semiconductor device as recited in Claim 23, further comprising metallization as the anode coupling means to the semiconductor die. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 35 includes the packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the anode to the semiconductor die, a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 37 includes the packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in an integrated circuit. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 38 includes the packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in a surface mount assembly. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 39 includes the packaged semiconductor device as recited in Claim 20, having length and width dimensions of approximately .079 millimeters and .050 millimeters, respectively, and a height dimension of approximately .032 millimeters. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 40 includes a packaged semiconductor device, comprising a light emitting semiconductor, a substrate, a terminal, and an encapsulant material. The light emitting semiconductor is disposed in the substrate, and a means for coupling the terminal to the light emitting semiconductor is provided. The terminal further comprising a terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range. A substantially clear encapsulant encapsulates the light emitting semiconductor, the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A,

6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 41 includes the packaged semiconductor device as recited in Claim 40, adapted for use in a surface mount assembly. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 42 includes a packaged semiconductor device, comprising a semiconductor die, a substrate and a plurality of leads, wherein at least one said lead has a shaped end configured to minimize parasitic capacitance over a predetermined frequency range. The semiconductor die is disposed on the substrate. A coupling means extends from the plurality of leads to the semiconductor die for providing low capacitance electrical connections which supports device functionality. An encapsulation material surrounds the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

Claim 43 includes the packaged semiconductor device as recited in Claim 42, adapted for use in a surface mount assembly. By way of example and not by limitation, see Figures 1-3, 5A, 5B, 5C, 6A, 6B, 6C, 7B and 8 of US2002/0121683 and the accompanying discussion thereof at paragraphs [0018]-[0025].

VI GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL (37 C.F.R. §41.37(c)(6))

1. Whether the Examiner has Failed to Properly Consider the Specification in Rejecting Claims 1-18, 20-35, and 37-43 for Failing to Comply with the Written Description Requirement.

2. Whether the Examiner has Failed to Properly Construe Claims 10 and 39 and 40-41.

3. Whether Claims 1-8, 12, 13, 15-18 and 42-43 are Anticipated by or Obvious in View of Nakayama.

4. Whether Claims 20-27, 29-32, 34-35, 37-38 and 40-41 are Unpatentable over Nakayama in view of Ishinaga.

5. Whether Claim 9 is Unpatentable over Nakayama in view of Crowley.

6. Whether Claims 28 and 33 are Unpatentable over Nakayama in view of Ishinaga and Further in View of Crowley.

VII ARGUMENTS (37 C.F.R. 41.37(c)(7))

1. The Examiner has Failed to Properly Consider the Specification in Rejecting Claims 1-18, 20-35, and 37-43 for Failing to Comply with the Written Description Requirement.

Claims 1-18, 20-35 and 37-43 stand rejected under 35 U.S.C. 112 as failing to comply with the written description requirement. In particular, the Examiner asserts in the Final Office action mailed July 25, 2006 that there is no support in the specification for the limitations in claim 1 of "said lead has a (1) shaped end proximate the substrate and configured to minimize parasitic capacitance over a predetermined frequency range" and "the (2) encapsulant having a consistent dielectric constant over the predetermined frequency range," for the limitation in claim 40 of "the (1) terminal shaped end configured to minimize parasitic capacitance over a predetermined frequency range," and for the limitations of claim 42 of "said (1) lead has a shaped end configured to minimize parasitic capacitance over a predetermined frequency range" and "the (2) encapsulant material having a consistent dielectric constant over the predetermined frequency range." (Reference numbers added).

Referring to US2002/0121683 at paragraph [0019], lines 1-6 that the "(1) bond wires are maintained at a minimal length and the (2) dielectric constant of the encapsulant material 12 is selected such that the performance of the device 10 is predictable, therefore (1, 2) enhancing the ability of the device 10 to minimize unwanted parasitics as the frequency of operation of signals coupled to the input terminal 14 increases." Furthermore, at paragraph [0021], lines 4 to 6, it is noted that "since the (2) parasitic capacitance is a function of dielectric constant of the encapsulant material 12, its performance is further improved and more predictable." Likewise, at paragraph [0024], lines 15 to 16 it is noted that the "(1) anode 71 has a shaped end surface operable to minimize parasitic capacitance," and at lines 21 to 23 it is noted that the "(1) bond wire 22 could have a length comprising a fraction of the wavelength for which frequency the semiconductor device 70 is designed." Likewise, as noted at paragraph [0005], lines 9-11, limiting the length of the bond wire to a fraction of a wavelength of the operating frequency limits the effect of parasitics. As support for the claim limitations of claims 1-18, 20-35 and 37-43 that were rejected under 35 U.S.C. 112 as failing to comply with the written description requirement has been clearly demonstrated to be present in the specification, the rejection of these claims must be REVERSED.

2. **The Examiner has Failed to Properly Construe Claims 10 and 39 and 40-41.**

The construction of the claims adopted by the Examiner is incorrect, and is used to improperly reject the claims. Claim construction is a question of law, and is reviewed *de novo*. *Markman v. Westview*, 52 F. 3d 967, 34 USPQ2d 1321 (Fed. Cir. 1995), *aff'd* 116 S.Ct. 1384 (1996).

Claim 10 includes the "packaged semiconductor device as recited in Claim 8, further comprising length and width dimensions of approximately .079 millimeters and .065 millimeters, respectively, and a height dimension of approximately .032 millimeters." Referring to Figures 3 and 4 of the Application, it is clear which dimensions are being claimed. The exemplary embodiment of semiconductor device package 10 has a length dimension of .079 millimeters (Figure 3), a width dimension of 0.64 millimeters, and a height dimension of 0.032 millimeters. No embodiments are shown in which semiconductor device package 10 has a width dimension of approximately 0.079 millimeters or 0.032 millimeters, and no embodiments are shown in which semiconductor device package 10 has a height dimension of approximately 0.079 millimeters or 0.065 millimeters. While such exemplary embodiments do not limit the broader claims that claim 10 depends from, such that they cover devices having other dimensions, when properly construed in light of the exemplary embodiments disclosed in the specification, claim 10 is not indefinite and the rejection of claim 10 must be REVERSED.

Likewise, claim 39 includes the "packaged semiconductor device as recited in Claim 20, having length and width dimensions of approximately .079 millimeters and .050 millimeters, respectively, and a height dimension of approximately .032 millimeters." As noted above, when construed in light of the exemplary embodiments claim 39 is not indefinite. The reference to the width dimension of 0.050 millimeters is shown in regards to encapsulant material 12, and Figures 7A-7D, 8A-8C and A-9C each show exemplary embodiments where the width, height and length dimensions claimed are clearly shown. As such, claim 39 is not indefinite and the rejection of claim 39 must be REVERSED.

In response to the rejection of claim 40, an amendment was presented in a Response to the Final Office Action to provide antecedent basis for the term "the terminal shaped end." The Examiner refused to enter the proposed amendment, stating that the "extensive changes to the claim 40 would require search and reconsideration of the proposed amended claim." It is clear

that providing antecedent basis for the term "the terminal shaped end" in the manner proposed by the Applicants was not an "extensive" change and would not require any additional search. The Applicants request entry of the proposed claim amendment, after which the rejection of claim 40 should be REVERSED.

3. Claims 1-8, 12, 13, 15-18 and 42-43 are not Anticipated by or Obvious in View of Nakayama, as it Fails to Disclose Each Element of the Claimed Invention.

Claim 1 includes a "packaged semiconductor device, comprising: a semiconductor die; a substrate with the semiconductor die disposed therein; a plurality of leads coupled to the semiconductor die, wherein at least one said lead has a shaped end proximate the substrate and configured to **minimize** parasitic **capacitance** over a predetermined frequency range; an encapsulant enclosing the semiconductor die and plurality of leads, the encapsulant having a consistant **dielectric** constant over the predetermined **frequency range**; and the encapsulant operable to shunt thermal capacitance and thermal resistance away from the semiconductor die." (Emphasis added). Nakayama fails to disclose at least a lead having a shaped end to minimize parasitic capacitance over a predetermined frequency range and an encapsulant having a consistent dielectric constant over a predetermined frequency range, which are disclosed in the specification of the pending application as described above. For example, Nakayama does not even contain the terms "dielectric," "capacitance," "minimize," or "frequency range." The Examiner asserts that leads 15 of Nakayama are "inherently configured to minimize parasitic capacitance." In order for inherency to provide a basis for rejection, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original) (Applicant's invention was directed to a biaxially oriented, flexible dilation catheter balloon (a tube which expands upon inflation) used, for example, in clearing the blood vessels of heart patients). The examiner applied a U.S. patent to Schjeldahl which disclosed injection molding a tubular preform and then injecting air into the preform to expand it against a mold (blow molding). The reference did not directly state that the end product balloon was biaxially oriented. It did disclose that the balloon was "formed from a thin flexible inelastic, high tensile strength, biaxially oriented synthetic plastic material." *Id.* at 1462 (emphasis in original). The examiner argued that Schjeldahl's balloon was inherently biaxially oriented. The Board reversed on the basis that the examiner did not provide objective evidence or cogent technical reasoning to support the conclusion of inherency.).

In this case, the Examiner has not provided any basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. A review of the leads 15 of Nakayama reveals why – there is simply no basis in fact or technical reasoning to support such a determination. The leads 15 of Nakayama are all rectangular, with sharp corners. As taught in the specification of the pending application at paragraph [0024], the "anode 71 has a shaped end surface operable to minimize parasitic capacitance." That shaped end surface noticeably contains no sharp corners. Thus, the Examiner has not only failed to provide any basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of Nakayama, he is unable to do so, as it is well-known that sharp corners increase the electric field gradient and thus the parasitic capacitance. While Nakayama discusses reduction of parasitic capacitance, there is no discussion whatsoever of parasitic capacitance.

Furthermore, in regards to the claim limitation "the encapsulant having a consistant **dielectric** constant over the predetermined **frequency range**," the Examiner fails to even address that limitation or assert that it is disclosed in Nakayama, inherently or otherwise. Nakayama does not discuss or even mention the dielectric constant of the molding resin 17. Accordingly, as the Examiner has failed to provide any basis in fact and/or technical reasoning to reasonably

support the determination that the one of the allegedly inherent characteristics necessarily flows from the teachings of Nakayama and has failed to even address a second claim limitation, the rejection of claim 1 must be REVERSED.

Claims 2, 3, 4, 5, 6, 7, 11 and 14 are allowable at least for the reason that they depend from an allowable base claim, and the rejection of these claims must be REVERSED.

Claim 8 includes "the packaged semiconductor device as recited in Claim 3, further comprising an end surface of the input terminal(s) being positioned adjacent and parallel to the side surface of the I/O common terminal, and an end surface of the output terminal(s) being positioned adjacent and parallel to the opposing side surface of the I/O common terminal, said end surfaces being shaped so as **to minimize parasitic capacitance**." (Emphasis added). In addition to the exemplary embodiment of anode 71 of the pending application discussed above, the specification discloses at paragraph [0021] that since "the bond wires 20 and 22 are kept short, package performance from one device to another is more consistent compared to SOT 23 and SOD 323 type packages. Also, since the parasitic capacitance is a function of dielectric constant of the encapsulant material 12, its performance is further improved and more predictable. The input and output terminals 14 the 16 are not parallel to each other, therefore avoiding parallel conductive surfaces which could create unwanted parasitics. Also, the input 14 and output 16 terminals have a rounded portion 24 and 26 which allow the length of the bond wires 20, 22 to be relatively short and further improves the performance of the device 10." In addition to terminal designs that avoid all sharp edges to minimize parasitic capacitance, additional exemplary embodiments are disclosed that minimize parasitic capacitance and which are not present in Nakayama. In regards to claim 8, the Examiner does not rely on inherency and asserts that such features are shown in Figures 1A-1C of Nakayama, but a cursory review of the differences between the rectangular leads 15 of Nakayama shows that they do not incorporate any of the features disclosed in the specification that are utilized to minimize parasitic capacitance, which are equally applicable to claims 1 and 8. As such, the rejection of claim 8 must be REVERSED.

In regards to claims 12, 13, 15 and 17, these claims are allowable at least for the reason that they depend from an allowable base claim, and the rejection of these claims must be REVERSED.

Claim 16 includes the "packaged semiconductor device as recited in Claim 15, further comprising a path length from input terminal to the output terminal, **<u>of a fraction of the wavelength for which frequency the semiconductor device is designed</u>**." (Emphasis added). Likewise, claim 18 includes the "packaged semiconductor device as recited in Claim 17, further comprising a path length from the input terminal to the output terminal **<u>of a fraction of the wavelength for which frequency the semiconductor device is designed</u>**." (Emphasis added). The Examiner asserts that this is disclosed at col. 11, lines 12-15 of Nakayama, which state in full that "Consequently, the radio frequency integrated circuit incorporated in the semiconductor chip 11 can be operated stably over a wide frequency region ranging from DC to radio frequency without receiving any thermal damage." As the wavelength of Nakayama is not specified, it fails to disclose the claim limitation of a "path length from input terminal to the output terminal, of a fraction of the wavelength for which frequency the semiconductor device is designed." In fact, Nakayama discloses no dimensions for the subject path length, only that parasitic inductance is reduced so as to allow operation over a wide frequency range without thermal damage. Such inductance-related losses from operation over a wide frequency range would not be present in a device operating at a fixed frequency of operation. Likewise, nothing in Nakayama indicates that the frequency of operation should be limited so as to limit a path length from input terminal to the output terminal to a fraction of the wavelength for which frequency the semiconductor device is designed. As such, the rejection of claims 16 and 18 must be REVERSED.

Claim 42 includes a "packaged semiconductor device, comprising: a semiconductor die, a substrate and a plurality of leads, wherein at least one said lead has a shaped end configured to minimize parasitic capacitance over a predetermined frequency range; the semiconductor die being disposed on the substrate; **<u>a coupling means extending from the plurality of leads to the semiconductor die for providing low capacitance electrical connections which supports device functionality</u>**; and an encapsulation material surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range." (Emphasis added). As discussed above, the structure disclosed in the specification includes that the path length from input terminal to the output terminal is a fraction of the wavelength for which frequency the semiconductor device is designed. The Examiner fails to address this structural

limitation or to construe the claim element under 35 U.S.C. 112(6), and as such, must be REVERSED.

Claim 43 is allowable at least for the reason that it depends from an allowable base claim, and the rejection of claim 43 must be REVERSED.

4. Claims 20-27, 29-32, 34-35, 37-38 and 40-41 are not Unpatentable over Nakayama in view of Ishinaga, Because they Fail to Disclose Each Element of the Claimed Inventions.

The Examiner rejects claims 20-27, 29-32, 34-35, 37-38 and 40-41 over Nakayama in view of Ishinaga using improper hindsight – since Nakayama fails to disclose a light emitting semiconductor, the Examiner used claims 20-27, 29-32, 34-35, 37-38 and 40-41 as a roadmap for selecting a reference that discloses a light-emitting semiconductor, Ishinaga. However, this combination actually weakens the Examiner's rejection of these and the other claims. Ishinaga, like Nakayama, fails to even mention the dielectric constant of the encapsulant, much less that it should be consistent over a predetermined frequency range. One would expect that out of the thousands of patents that disclose a light-emitting semiconductor, the Examiner could find at least one that addresses the dielectric constant of the encapsulant, but apparently none exist.

Furthermore, claims 20-27, 29-32, 34-35, 37-38 and 40-41 include more than just the combination of a light-emitting semiconductor with the the packaged semiconductor device as recited in Claim 1. For example, claim 22 includes the packaged semiconductor device as recited in Claim 20, further comprising **a substantially clear epoxy material as the encapsulant**. Hence, not only must the encapsulant have a consistent dielectric constant over the predetermined frequency range, it must also be substantially clear. The failure of either Nakayama or Ishinaga to disclose an encapsulant having a consistent dielectric constant over the predetermined frequency range, much less the effect that the color of the encapsulant must be taken into consideration, makes it clear that the rejection of claim 22 must be REVERSED.

Likewise, claim 40 includes "a packaged semiconductor device, comprising: a light emitting semiconductor, a substrate, a terminal, and an encapsulant material; the light emitting semiconductor being disposed in the substrate; **a means coupling the terminal to the light emitting semiconductor**; the terminal further comprising a terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range; a substantially clear

encapsulant for encapsulating the light emitting semiconductor, the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance." (Emphasis added). The Examiner has failed to address the means-plus-function limitation of claim 40 under 35 U.S.C. 112(6) and the structural limitations disclosed in the specification and described above that are not present and for which there is no equivalent in either Nakayama or Ishinaga. As such, the rejection of claim 40 must be REVERSED.

Claims 20, 21, 23-27, 29-32, 34-35, 37-38 and 41 are allowable at least for the reason that they depend from an allowable base claim, and the rejection of these claims must be REVERSED.

5. Claim 9 is not Unpatentable over Nakayama in view of Crowley, as they Fail to Disclose Each Element of the Claimed Invention.

Claim 9 includes the packaged semiconductor device as recited in Claim 1, wherein the configured lead has a rounded shape expanding outward toward the substrate. The Examiner admits that Nakayama discloses this limitation, but asserts that it is disclosed as leadframe terminal 38 of Crowley. As an initial matter, it is curious that the Examiner should admit that such a rounded shape is absent from Nakayama in regards to claim 9, but assert that it is inherently present in the rejection of claim 1 over Nakayama under 35 U.S.C. 102, or that it is present in the combination of Nakayama in view of Ishinaga in the rejection of claim 42, where the structure corresponding to the means-plus-function limitation "a coupling means" is not addressed. Nevertheless, leadframe terminal 38 of Crowley fails to disclose a configured lead that has a rounded shape expanding outward toward the substrate – at best, it appears that the corners of leadframe terminal 38 have been rounded, although there is no description of any such rounded corners of leadframe 38 in Crowley. Regardless of what is shown and not described in Crowley, rounded corners of a leadframe are not a configured lead that has a rounded shape expanding outward toward the substrate, such as shown in Figures 1, 2, 5a and 6a of the pending application. The rounded corners of leadframe terminal 38 of Crowley are just that – a lead with rounded corners. There is no rounded shape expanding toward the substrate disclosed in Crowley, and the rejection of claim 9 must be REVERSED.

6. Claims 28 and 33 are not Unpatentable over Nakayama in view of Ishinaga and Further in View of Crowley, as they Fail to Disclose Each Element of the Claimed Invention.

Again using the claims as a road map, the Examiner rejects claims 28 and 33 over the combination of cited art, and again, this combination demonstrates that failure of the cited art to disclose each element of the claimed invention. While Crowley also discloses an encapsulated circuit, there is again no mention that the encapsulant has a consistant dielectric constant over a predetermined frequency range. As with Nakayama and Ishinaga, Crowley fails to even mention the dielectric constant of the encapsulant. Out of the thousands of patents disclosing encapsulated circuits, the Examiner was unable to find a single reference that discloses an encapsulant having a consistant dielectric constant over a predetermined frequency range. Likewise, Crowley also fails to disclose at least one lead that has a shaped end proximate the substrate and configured to minimize parasitic capacitance over a predetermined frequency range. In fact, he word "parasitic" is not even used in Crowley, again establishing that the apparent rounded corners of leadframe terminal 38 of Crowley were shown as such because of a draftsperson's artistic license rather than out of any intention to minimize parasitic capacitances. As such, the rejection of claims 28 and 33 must be REVERSED.

VIII APPENDIX OF CLAIMS (37 C.F.R. 41.37(c)(8))

The text of the claims involved in the appeal are:

1. A packaged semiconductor device, comprising:

a semiconductor die;

a substrate with the semiconductor die disposed therein;

a plurality of leads coupled to the semiconductor die, wherein at least one said lead has a shaped end proximate the substrate and configured to minimize parasitic capacitance over a predetermined frequency range;

an encapsulant enclosing the semiconductor die and plurality of leads, the encapsulant having a consistant dielectric constant over the predetermined frequency range; and

the encapsulant operable to shunt thermal capacitance and thermal resistance away from the semiconductor die.

2. The packaged semiconductor device as recited in Claim 1, further comprising an I/O common terminal, at least one input terminal and at least one output terminal, coupled to the semiconductor die.

3. The packaged semiconductor device as recited in Claim 2, wherein the input terminal(s) and output terminal(s) are positioned orthogonal to the I/O common terminal.

4. The packaged semiconductor device as recited in Claim 3, wherein the semiconductor die is positioned above the I/O common terminal.

5. The packaged semiconductor device as recited in Claim 4, wherein the encapsulant forms a substantially hexagonal structure surrounding the I/O common terminal, input terminal(s), and output terminal(s), essentially at right angles with respect to the substrate.

6. The packaged semiconductor device as recited in Claim 5, further comprising a lead-frame for coupling the input terminal(s) to a circuit and the output terminal(s) to a circuit.

7. The packaged semiconductor device as recited in Claim 6, wherein the portion of the lead-frame coupled to each of the input terminal(s) and output terminal(s) possess exposed dovetailed side edges operable to allow epoxy to lock on the sides and top of the exposed edges.

8. The packaged semiconductor device as recited in Claim 3, further comprising an end surface of the input terminal(s) being positioned adjacent and parallel to the side surface of the I/O common terminal, and an end surface of the output terminal(s) being positioned adjacent and parallel to the opposing side surface of the I/O common terminal, said end surfaces being shaped so as to minimize parasitic capacitance.

9. The packaged semiconductor device as recited in Claim 1, wherein the configured lead has a rounded shape expanding outward toward the substrate.

10. The packaged semiconductor device as recited in Claim 8, further comprising length and width dimensions of approximately .079 millimeters and .065 millimeters, respectively, and a height dimension of approximately .032 millimeters.

11. The packaged semiconductor device as recited in Claim 8, further comprising an operating frequency range from DC to 10 gigahertz.

12. The packaged semiconductor device as recited in Claim 8, further comprising use in a surface mount assembly.

13. The packaged semiconductor device as recited in Claim 8, further comprising use in an integrated circuit.

14. The packaged semiconductor device as recited in Claim 8, further comprising use in an amplifier gain stages.

15. The packaged semiconductor device as recited in Claim 8, further comprising metallization, including a first and second metallization strip, as the means of coupling the input terminal(s) and the output terminal(s) to the semiconductor die.

16. The packaged semiconductor device as recited in Claim 15, further comprising a path length from input terminal to the output terminal, of a fraction of the wavelength for which frequency the semiconductor device is designed.

17. The packaged semiconductor device as recited in Claim 8, further comprising bond wires as the means of coupling the input terminal(s) and the output terminal(s) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire, a second end of the first bond wire being coupled to the semiconductor die, a first end of a second bond wire being coupled to the semiconductor die, a second end of the second bond wire being coupled to the output terminal.

18. The packaged semiconductor device as recited in Claim 17, further comprising a path length from the input terminal to the output terminal of a fraction of the wavelength for which frequency the semiconductor device is designed.

20. The packaged semiconductor device as recited in Claim 1, further comprising a light emitting semiconductor as the semiconductor die.

21. The packaged semiconductor device as recited in Claim 20, further comprising a light emitting diode as the light emitting semiconductor.

22. The packaged semiconductor device as recited in Claim 20, further comprising a substantially clear epoxy material as the encapsulant.

23. The packaged semiconductor device as recited in Claim 20, further comprising a cathode and an anode as the plurality of leads.

24. The packaged semiconductor device as recited in Claim 23, further comprising the positioning of the cathode and the anode opposite to each other.

25. The packaged semiconductor device as recited in Claim 24, further comprising an encapsulant with a substantially hexagonal structure around the cathode and the anode essentially at right angles with respect to the substrate.

26. The packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the cathode.

27. The packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the cathode operable to minimize parasitic capacitance.

28. The packaged semiconductor device as recited in Claim 27, further comprising a rounded shape on the end surface of the cathode.

29. The packaged semiconductor device as recited in Claim 23, further comprising metallization as the cathode coupling means to the semiconductor die.

30. The packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the cathode to the semiconductor die, a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die.

31. The packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the anode.

32. The packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the anode operable to minimize parasitic capacitance.

33. The packaged semiconductor device as recited in Claim 32, further comprising a rounded shape on the end surface of the anode.

34. The packaged semiconductor device as recited in Claim 23, further comprising metallization as the anode coupling means to the semiconductor die.

35. The packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the anode to the semiconductor die, a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die.

37. The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in an integrated circuit.

38. The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in a surface mount assembly.

39. The packaged semiconductor device as recited in Claim 20, having length and width dimensions of approximately .079 millimeters and .050 millimeters, respectively, and a height dimension of approximately .032 millimeters.

40. A packaged semiconductor device, comprising:

a light emitting semiconductor, a substrate, a terminal, and an encapsulant material;

the light emitting semiconductor being disposed in the substrate;

a means coupling the terminal to the light emitting semiconductor;

the terminal further comprising a terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range;

a substantially clear encapsulant for encapsulating the light emitting semiconductor, the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

41. The packaged semiconductor device as recited in Claim 40, adapted for use in a surface mount assembly.

42. A packaged semiconductor device, comprising:

a semiconductor die, a substrate and a plurality of leads, wherein at least one said lead has a shaped end configured to minimize parasitic capacitance over a predetermined frequency range;

the semiconductor die being disposed on the substrate;

a coupling means extending from the plurality of leads to the semiconductor die for providing low capacitance electrical connections which supports device functionality; and

an encapsulation material surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range.

43. The packaged semiconductor device as recited in Claim 42, adapted for use in a surface mount assembly.

IX EVIDENCE APPENDIX (37 C.F.R. 41.37(c)(9))

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X RELATED PROCEEDINGS APPENDIX (37 C.F.R. 41.37(c)(10))

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Dated: January 22, 2007

Respectfully submitted,

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